UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,348	07/27/2001	Tomoya Kodama	212091US2SRD	7192

22850 7590 04/06/2006

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
CHAU, COREY P	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,348	KODAMA, TOMOYA	
	Examiner	Art Unit	
	Corey P. Chau	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 6-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 15-19, 21-23, 25-29 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6275239 to Ezer et al. (hereafter as Ezer).

3. Regarding Claim 15, Ezer discloses a data processing apparatus for processing an input data stream via an external memory (103) comprising:

a control processor(101) to fetch in a program and data to be used for a next procedure of an audio process from programs for encoding and decoding, input/output data, work data, table data which are stored in the external memory (Figs. 5 and 6);

a coprocessor (102) to subserve the control processor to perform data processing for coding or decoding sequentially, according to the program fetched by the control processor (abstract; Figs. 1, 2, 8, and 9; column 1, line 60 to column 2, line 31);

a data memory (407) to store the data fetched by the control processor;

an instruction memory (405) to store the control programs to be applied to the processor; and

a DMA controller (104,411) to transfer the data among the instruction memory and the data memory and the external memory (Fig. 4),

the control processor controlling the DMA controller to perform the encoding and the decoding using the coprocessor, read program and data required for the next procedure from the external memory, and write data obtained by the procedure into the external memory (Figs. 4 and 6).

4. Regarding Claim 16, Ezer discloses the coprocessor temporally stops when accessing of the DMA controller to the instruction memory or the data memory competes with accessing of the coprocessor to the instruction memory or the data memory (Fig. 4).

5. Claim 17 is essentially similar to Claim 1 and is rejected for the same reasons stated above apropos to Claim 1.

6. Claim 18 is essentially similar to Claim 2 and is rejected for the same reasons stated above apropos to Claim 2.

7. Regarding Claim 19, Ezer discloses an audio data processing method comprising:

storing a plurality of program modules corresponding to the plurality of procedures and data to be processed in an external memory (103);

reading, when executing one process, a program module and to be processed data which are used for a next procedure of the audio process from the external memory a control processor (101); and

subjecting audio data of the readout data sequentially to procedures of an audio process via a coprocessor (102) in accordance with the readout program module (Figs. 2, and 7-9).

8. With regards to Claims 21-23, while Ezra discloses that the coprocessor is applicable to audio and video data, Ezra does not disclose that the coprocessor is configured to process only audio data. Examiner takes official notice that it is well known to utilize a system capable of processing audio and video data to process only audio data. Therefore, it would have been obvious to one of ordinary skill to modify the system of Ezra to process only audio data in an audio-only environment.

9. Regarding Claim 25, Ezer discloses at least two parallel busses lead from the instruction memory and the data memory to the coprocessor (Fig. 4).

10. Regarding Claim 26, Ezer discloses said fetching further comprises: transferring the programs and the audio data by at least two parallel busses from the internal memory to the coprocessor (Fig. 4).

11. Regarding Claim 27, Ezer discloses said storing the program and the audio data in the internal memory, the audio data is stored to a data memory, and the programs are stored to an instruction memory (Fig. 4).

12. Regarding Claim 28, Ezer discloses said reading further comprises: storing the program module and the to-be-processed data from the external memory (103) to an internal memory (Figs. 2 and 4); and transferring the program module and the to-be-processed data by at least two parallel busses from the internal memory to the coprocessor (Figs. 2 and 4).

13. Regarding Claim 29, Ezer discloses the internal memory includes an instruction memory (405) and a data memory (407), and wherein said storing, the to-be-processed data is stored to the data memory and the program module is stored to the instruction memory (Fig. 4).

14. Regarding Claim 31, Ezer discloses an audio input/output interface (Fig. 1); and an internal bus; wherein the internal bus links the control processor, the coprocessor and the audio input/output interface together (Figs. 2 and 4).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1-3, 6-14, 20, 24, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6275239 to Ezer.

17. Regarding Claim 1, Ezer discloses an audio processor which processes an input data stream via an external memory (103)(Fig. 1), comprising:

a control processor (101) to fetch in, when executing one of divided procedures of an audio process, a program and audio data corresponding to a next one of the procedures from the external memory (103) which stores programs and a group of data used for sequentially executing the divided procedures of the audio process (Figs. 5 and 6);

an internal memory (405,407,416,425)(Fig. 4; claim 6) to store the program and audio data fetched from the external memory by the control processor and corresponding to the one and the next one of the procedures;

a coprocessor (102) to subserve the control processor to subject audio data of the input data stream to the divided procedures of the audio process sequentially (abstract; Figs. 8 and 9), based on the program fetched by the control processor (Figs. 1 and 2; column 1, line 60 to column 2, line 31).

Ezer does not expressly disclose the coprocessor executing multiplication/accumulation addition according to VLIW (Very Long Instruction Word). However, Examiner takes Official Notice that it would have been obvious to one having ordinary skill in the art to have the coprocessor execute multiplication/accumulation, addition according to VLIW (Very Long Instruction Word), wherein one VLIW instruction encodes multiple operations and therefore multiple operations can be handled at the same time, resulting in faster processing. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Ezer to have the coprocessor execute multiplication/accumulation, addition according to VLIW (Very Long Instruction Word), wherein one VLIW instruction encodes multiple operations and

therefore multiple operations can be handled at the same time, resulting in faster processing.

18. Regarding Claim 2, Ezer as modified discloses the coprocessor is configured to subserve the control processor to subject sequentially the audio data to decoding, noise-less decoding, noise reduction, filter bank, and block switching in accordance with the programs and data fetched from the external memory in units of one procedure (Figs. 8 and 9; column 10, line 41 to column 11, line 42).

19. Regarding Claim 3, Ezer as modified discloses the coprocessor (102) is configured to subserve the control processor to execute the program fetched in the internal memory from the external memory in accordance with progress of the procedures of the audio process (Fig. 4).

20. Regarding Claim 6, Ezer as modified discloses the internal memory comprises an instruction memory (405) configured to store an instruction group of the program transferred from the external memory and a data memory (407) configured to store a data group transferred from the external memory, and the coprocessor subserves the control processor to perform the process based on the instruction group using the data in the data memory and data corresponding to a progress stage of audio data reconstruction to generate audio data (Fig. 4).

21. Regarding Claim 7, Ezer as modified discloses a DMA controller (104,411) configured to control writing of data to the external memory, the instruction memory and the data memory, and reading of the data therefrom by a direct access memory transfer (Figs. 1 and 4).

22. Regarding Claim 8, Ezer as modified discloses the control processor sequentially transfers a plurality of program modules corresponding to procedures of the audio process to the coprocessor from the external memory according to the progress of the procedures (Figs. 1 and 2; column 1, line 60 to column 2, line 31).

23. Regarding Claim 9, Ezer as modified discloses the coprocessor (102) subserves the control processor to execute decoding of bit stream data, noiseless decoding, inverse quantization, scale factor, TNS processing, filter bank processing, and the block switching, in this order, to reconstruct audio data (Figs. 8 and 9; column 10, line 41 to column 11, line 42).

24. Regarding Claim 10, Ezer as modified discloses the control processor includes a function of predicting which procedure is performed after the procedure which is currently performed (Figs. 4 and 6).

25. Regarding Claim 11, Ezer as modified discloses the internal memory stores a program module which request the DMA controller for preparing, while continuing the procedure which is currently performed, the data group and instruction group that are required for the next procedure (Figs. 4 and 6).

26. Regarding Claim 12, Ezer as modified discloses wherein a DMA transfer instruction is added to the program module in order to read the program module used in the next procedure from the external memory, the DMA transfer instruction allowing to read the program module with the DMA transfer by specifying the storage area (Figs. 4 and 6).

27. Regarding Claim 13, Ezer as modified discloses the control processor is further configured to save data stored in the internal memory from the internal memory to the external memory if determine to be unused for a predetermined time by the control processor (Figs. 2, 4, 7, and 9).

28. Regarding Claim 14, Ezer as modified discloses the control processor is further configured to release a storage region of the internal memory occupied by the data stored in the internal memory or a program if the data stored in the internal memory or the program becomes unused by the coprocessor (Figs. 2, 4, 7, and 9).

29. With regards to Claim 20, while Ezra as modified discloses that the coprocessor is applicable to audio and video data, Ezra as modified does not disclose that the coprocessor is configured to process only audio data. Examiner takes official notice that it is well known to utilize a system capable of processing audio and video data to process only audio data. Therefore, it would have been obvious to one of ordinary skill to modify the system of Ezra as modified to process only audio data in an audio-only environment.

30. Regarding Claim 24, Ezer as modified discloses the internal memory includes an instruction memory and a data memory, and at least two parallel busses lead from the instruction memory and the data memory to the coprocessor (Fig. 4).

31. Regarding Claim 30, Ezer as modified discloses an audio input/output interface (Fig. 1); and an internal bus; wherein the internal bus links the control processor, the coprocessor and the audio input/output interface together (Figs. 4).

Response to Arguments

32. Applicant's arguments filed 12/23/2005 have been fully considered but they are not persuasive.

33. With respect to Applicant's argument on page 13, stating that "Ezer does not teach or suggest the control processor to fetch in, when executing one of divided procedures of an audio process, ***a program and audio data corresponding to a next one of the procedures from the external memory***", has been noted. However, the Examiner respectfully disagrees. Ezer discloses the MSP Instruction Memory (Imem) reads code for the next function to be performed from a task list updated by the CPU, wherein in the task list is contain in the DRAM, which reads on the control processor to fetch in, when executing one of divided procedures of an audio process, ***a program and audio data corresponding to a next one of the procedures from the external memory***. See Figs. 2 and 7; column 9, line 44 to column 10, line 40.

34. Applicant's arguments with respect to claims 1-3, 6-14, 20, 24, and 30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

35. The Art Unit location of your application in the USPTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Division 2615

36. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey P. Chau whose telephone number is (571)272-7514. The examiner can normally be reached on Monday - Friday 9:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chin Vivian can be reached on (571)272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 3, 2006
CPC

VIVIAN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

4/03/06